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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI-29058
First Named Inventor or Application Identifier	Mandy Mei-Feng Tsai
Title	Interface Between Different Clock Rate Components
Express Mail Label No.	EL360244241

jc526 U.S. PTO 09/535226 03/24/00

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] *Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification *[Total Pages* 15 *]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC d113)* *[Total Sheets* 4 *]*
4. Oath or Declaration *[Total Pages* X *]*
   - a. [ ] Newly Executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR §1.63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: /

Prior application information: ***Examiner*** _____ ***Group / Art Unit:*** _____

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INTERFACE BETWEEN DIFFERENT CLOCK RATE COMPONENTS

CROSS-REFERENCE TO COPENDING APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/126,079, filed on March 25, 1999, the entire disclosure of which is hereby incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to digital signal processing. More particularly, the present invention relates to a method and a circuit for interfacing a low clock rate component with a high clock rate component.

BACKGROUND OF THE INVENTION

In the field of digital signal processing, the need for interfacing a low clock rate component with a high clock rate component is very common. For example, in a digital still camera, real-time data from a charge-coupled device (CCD) is transferred to a high speed memory, such as a synchronous dynamic random access memory (SDRAM). For these purposes, "real-time" means that data is transferred at a rate fast enough to avoid a perceivable delay in operation of the system, in this example, a digital still camera. The CCD operates at a clock rate of about 12 MHz, while the SDRAM operates at a clock rate of about 54 MHz. To smooth the transfer of the real-time data

flow, an interface between the low clock rate CCD and the high clock rate SDRAM is needed to accommodate the difference between the clock rates.

There are two primary prior art approaches for the interface of two components having different operating speeds: a First-In-First-out (FIFO) buffering configuration and a dual-port memory buffering configuration.

A diagram of a prior art FIFO configuration is shown in Fig. 1. FIFO comprises a memory 2 that is accessible by the data source 4 anytime there is space available and is accessible by the destination 6 anytime there is data available from the source. FIFO also comprises hardware control logic 8, such as a read/write access pointer controller, to control the access to the FIFO by both the data source and the destination so as to ensure that the data will be transferred correctly. In the case that the clock rate of the data source is higher than that of the destination, the control logic must detect when the memory of the FIFO is full and send a signal to the data source, if the memory is detected as full, to hold the data transmitted from the source until the memory is detected as nearly empty. In the other case when the clock rate of the destination is higher than that of the data source, the control logic must detect when the memory of the FIFO is empty or nearly empty and send a signal to the destination, if the memory is detected as empty or nearly empty, to hold the access to the FIFO by the destination until the memory is detected as full. This operation requires relatively complex control logic and a relatively long timing delay, which slows down the performance of the component with the higher clock rate. Such a solution is practical only if using a slow clock source.

Dual-port memory circuits (i.e. a memory array accessible by two ports) are a more versatile form of time domain boundary buffer. The read and write operations of a dual-port buffer are based on address rather than write order, thereby allowing the reading of data in a different order than it was written in, for example. Lock-outs are used in a dual-port buffer to

prevent reading from a memory element while it is being written. Dual-port buffers can be arranged to not slow down the performance of the component with the higher clock rate if the read/write operations are coordinated properly. Unfortunately, the implementation of a dual-port buffer is more complicated than that of a FIFO and is difficult to integrate into an integrated circuit die. Hence, a dual port memory is typically used as a discrete component, adding to system size and complexity. In addition, the manufacturing costs of dual-port buffers are comparatively higher than single-port memory circuits.

There is therefore a need in the industry for a cost-effective interface solution that allows real-time data transfer between two components having different clock rates.

SUMMARY OF THE INVENTION

In one embodiment of the invention, a circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate, wherein the second clock rate is higher than the first clock rate, is disclosed. The circuit comprises a first buffer coupled to the first component; a second buffer coupled to the second component; and a copy/access controller connected to the first buffer, the second buffer, and the second component. The copy/access controller is operable to copy data from the first buffer to the second buffer when the first buffer is substantially full. It is also operable to prompt the second component to access the second buffer when the data is copied from the first buffer. The buffers can be random access memories or shift registers, and can be integrated onto the same semiconductor die as either the first or second component.

In another embodiment of the invention, a circuit for transferring a real-time data flow from a first component operable at a first clock rate to a second component operable at a second clock rate is disclosed, wherein the second clock rate is higher than the first clock rate. The circuit comprises a first clock signal source of the first clock rate; a second clock signal source of the second clock rate; a first buffer operable at either the first clock rate or the second clock rate and coupled to the first component and the second component; a second buffer operable at either the first clock rate or the second clock rate and coupled to the first component and the second component. The circuit also includes a clock switch coupled to the first buffer and to the second buffer and coupled to the first and second clock signal sources. The clock switch is operable to couple the first clock signal source to either the first buffer or the second buffer and is operable to couple the second clock signal source to the other of the first buffer and the second buffer when one of the buffers is substantially full.

An advantage of the invention is that it provides an interface between two different speed components using cost-effective single port memory circuits rather than dual port memories.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects and advantages of the present invention will become apparent from the following descriptions taken in conjunction with the accompanying drawings, wherein:

Figure 1 shows a prior art FIFO configuration;

Figure 2 shows a block diagram of a first embodiment of the present invention;

Figure 3 shows a block diagram of a clock switching circuit of said first embodiment of the present invention;

Figure 4 shows a block diagram of a second embodiment of the present invention; and

Figure 5 shows a block diagram of copy/access circuitry of said second embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

A ping-pong buffer generally comprises two memory elements that can be written to and read from alternately. In the usual situation, one memory element (e.g. the "ping" buffer) is filled with data while the other memory element (e.g. the "pong" buffer) has its data read by another component. This eliminates the delay that would occur if the incoming data, for example, had to be suspended while the data in the buffer is being read. The ability of ping-pong buffers to handle uninterrupted streams of data can be used as a solution for interfacing electronic components having two different operating speeds or clock rates.

Reference now will be made in detail to the preferred embodiments of the present invention as illustrated in the accompanying drawings in which like reference numerals designate like or corresponding elements throughout the drawings.

Fig. 2 illustrates a first embodiment of the present invention, wherein a ping-pong buffer 10 is used as an interface between a low clock rate component 11 (e.g. a CCD operable at about 12 MHz or a TV data output operable at 13.5 MHz) and a high clock rate component 12 (e.g. an SDRAM operable at about 54 MHz) in a real-time application. The ping-pong buffer 10 comprises a ping buffer 13, a pong buffer 14 and a clock switch 15. The buffers can be any size, such as 8 by 32-bits for example, and comprise a memory device such as a shift register comprising D Flip-Flops or a RAM. The clock rate of the ping buffer 13 can be switched between a clock signal source (not shown) at the clock rate of the component 11 and a clock signal source (not shown) at the clock rate of the component 12. The ping buffer 13 can be accessed by the component 11 if it is operating at the clock rate of the component 11, and it can be accessed by the component 12 if it is operating at the clock rate of the component 12. Access between the components 11 and

12 and the ping 13 and pong 14 buffers can be controlled using an address pointer controller 16 and a comparator 17. Similarly, the clock rate of the pong buffer 14 can also be switched between the clock rate of the component 11 and the clock rate of the component 12. And when the pong buffer 14 is operating at the clock rate of the component 11, it can be accessed by the component 11, while if it is operating at the clock rate of the component 12, it can be accessed by the component 12. The clock switch 15 is coupled to both the ping buffer 13 and the pong buffer 14 and switches between the clock sources.

In one example, the ping buffer 13 operates at the clock rate of the component 11 and is receiving a real-time data flow from the component 11. When the ping buffer 13 is full, the clock switch 15 switches from the clock signal source for the clock rate of the ping buffer 13 to clock signal source for the clock rate of the component 12 and switches the clock signal source for the clock rate of the pong buffer 14 to the clock signal source for the clock rate of the component 11, such that the component 12 can obtain the data from the ping buffer 13 and the pong buffer 14 can continue receiving the real-time data flow from the component 11. Similarly, when the pong buffer 14 is full, the clock switch 15 will again exchange the clock rates of the ping buffer 13 and the pong buffer 14 to let the component 12 obtain data from the pong buffer 14 and let the ping buffer 13 continue receiving real-time data flow from component 11.

To determine whether the ping buffer 13 or the pong buffer 14 is full or not, the ping-pong buffer 10 may include a counter. A predetermined number corresponding to the capacity of each of the ping buffer 13 and the pong buffer 14 is set in the counter. At first, the counter is set to zero. In addition, each time the clock rates of the ping buffer 13 and the pong buffer 14 are switched, the counter is reset to zero. When each vacancy of the ping buffer 13 or the pong buffer 14 is occupied by a datum from the component 11, the

counter is increased by one. When the counter reaches the predetermined number, the clock switch 15 executes the switching of the clock rates of the ping buffer 13 and the pong buffer 14. In some applications, the predetermined number may be set to correspond to the condition that the ping buffer 13 or the pong buffer 14 is nearly full but not completely full, to prevent the switching of clock rates from causing interruptions to the receiving of the real-time data flow. In brief, the switching of clock rates is executed when one of the ping buffer 13 and the pong buffer 14 that is receiving data from the component 11 is substantially full (i.e., the buffer is full or nearly full). In addition, the predetermined numbers corresponding to the capacities of the ping buffer 13 and the pong buffer 14 respectively may be different if the capacities of the ping buffer 13 and the pong buffer 14 are different.

Fig. 3 shows one method for switching between the components 11 and 12 and the buffers 13 and 14. The output of a pointer counter 16 indicates which buffer 13 or 14 is accessible by a component at a given time. Once the counter value is equal to the buffer size (as determined by comparator 17), the comparator issues a signal to switch 15 so that the component 11 or 12 can access the other buffer 13 or 14. The switch also reverses the connection of the two different clock sources to the buffers 13 and 14 at this time.

The circuit of the ping-pong buffer 10 of the present invention is much simpler than that of a FIFO or a dual-port buffer and can be more easily integrated onto the same semiconductor die as either the component 11 or the component 12. A reason for this is that in the ping-pong buffer approach, the components 11 and 12 do not require any status feedback from the ping or pong buffers. The buffer operation depends only on the passive counter and comparator logic. The components 11 and 12 can therefore read or write without stopping or slowing the data transfer to allow for status logic delay. Conversely, in the FIFO approach the FIFO and high and low clock rate

components handshake and operate in accordance with a FULL/EMPTY flag. Handshake logic is performed with decision circuits in both the FIFO and the high and low clock rate components, a more complex and space-consuming configuration than is required in the ping-pong buffer implementation. The dual-port memory approach suffers from the same complexity drawbacks, but also has the added disadvantage of the inherently higher cost of the memory itself.

Fig. 4 illustrates a second embodiment of the present invention wherein a ping-pong buffer 20 is used as an interface between a low clock rate component 21 and a high clock rate component 22. As compared with the first embodiment, the structure and mechanism of the second embodiment is further simplified because the clock switch is eliminated and each buffer need only be operable at a single clock rate. Operating a component at a single clock rate has the advantage of eliminating potential uncertainty that can result from phase delays between multiple clock sources.

The ping-pong buffer 20 of the second embodiment comprises a ping buffer 23, a copy/access controller 24 and a pong buffer 25. The ping buffer 23 is used for receiving data from the component 21 and operates at the clock rate of the component 21. The pong buffer 25 is accessed by the component 22 and operates at the clock rate of the component 22. When the ping buffer 23 is full, the copy/access controller 24 executes a copy operation to copy data from the ping buffer 23 to the pong buffer 25. When the copy operation is completed, the copy/access controller 24 sends a signal to the component 22 to let the component 22 obtain data from the pong buffer 25, and at the same time, the ping buffer 23 continues receiving data from the component 21. As with the first embodiment mentioned above, the second embodiment circuit can include a counter to indicate when the ping buffer 23 is full or nearly-full.

Fig. 5 is a schematic diagram of a copy/access controller. Access counter 27 is increased by one when data shifts from one D Flip-Flop 29 to the next D Flip-Flop 31 in ping buffer 23. Once data shifts to the end of the ping buffer (i.e. to D Flip-Flop 33), the counter 27 value is equal to the buffer size. Comparator 35 then generates a load signal to COPY logic 37 to allow the data in ping buffer 23 to be copied to pong buffer 25. The copy operation takes one cycle of the low clock signal.

In another embodiment of the invention, each of the ping buffer 23 and the pong buffer 25 of the second embodiment can be implemented by using a RAM. This approach is slightly more complicated since data addresses and data address logic are needed in the copy operation between the two memories.

The technical features and technical contents of the present invention have been fully disclosed as above. However, various modifications or replacements can be made by people skilled in the art based on the disclosure and teaching of the present invention without departing from the spirit of the present invention. Therefore, the scope of the present invention shall not be limited to the above-disclosed embodiments and should include these modifications and replacements.

What is claimed is:

1. A circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate wherein said second clock rate is higher than said first clock rate, said circuit comprising:

a first buffer coupled to said first component;

a second buffer coupled to said second component;

a copy/access controller connected to said first buffer, said second buffer, and said second component and operable to copy data from said first buffer to said second buffer when said first buffer is substantially full, and further operable to prompt said second component to access said second buffer when said data is copied from said first buffer.

2. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are random-access memories.

3. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are shift registers.

4. The circuit as set forth in Claim 1, wherein said circuit is integrated onto a semiconductor die with one of said first component or said second component.

5. A circuit for transferring a real-time data flow from a first component operable at a first clock rate to a second component operable at a second clock rate wherein said second clock rate is higher than said first clock rate, said circuit comprising:

a first clock signal source of said first clock rate;

a second clock signal source of said second clock rate;

a first buffer operable at either said first clock rate or said second clock rate and coupled to said first component and said second component;

a second buffer operable at either said first clock rate or said second clock rate and coupled to said first component and said second component;

a clock switch coupled to said first buffer and to said second buffer and coupled to said first and second clock signal sources, said clock switch being operable to couple said first clock signal source to either said first buffer or said second buffer and operable to couple said second clock signal source to the other of said first buffer and said second buffer when one of said buffers is substantially full.

6. The circuit as set forth in Claim 5, wherein said circuit is integrated onto the same semiconductor die as one of said first component or said second component.

7. A method for interfacing between a first component operable at a first clock rate and a second component operable at a second clock rate wherein said second clock rate is higher than said first clock rate, comprising the steps of:

transferring data from said first component to a first buffer operable at said first clock rate;

copying data from said first buffer to a second buffer operable at said second clock rate when said first buffer is substantially full; and

prompting said second component to access said data in said second buffer when said copying step is completed.

8. The method as set forth in Claim 7, wherein both said first buffer and said second buffer are shift-register structures.

9. The method as set forth in Claim 7, wherein both said first buffer and said second buffer are random access memories.

10. The method as set forth in Claim 7, wherein said first buffer and said second buffer are both integrated onto the same semiconductor die as one of said first component or said second component.

ABSTRACT

A circuit for interfacing between a first component 11 operating at a first clock rate and a second component 12 operating at a second clock rate, wherein the second clock rate is higher than the first clock rate. The circuit comprises a first buffer 13 coupled to the first component 11; a second buffer 14 coupled to the second component 12; and a copy/access controller 15, 16, 17 connected to the first buffer 13, the second buffer 14, and the second component 12. The copy/access controller 15, 16, 17 is operable to copy data from the first buffer 13 to the second buffer 14 when the first buffer 13 is substantially full. It is also operable to prompt the second component 12 to access the second buffer 14 when the data is copied from the first buffer 13. The buffers can be random access memories or shift registers, and can be integrated onto the same semiconductor die as either the first or second component.

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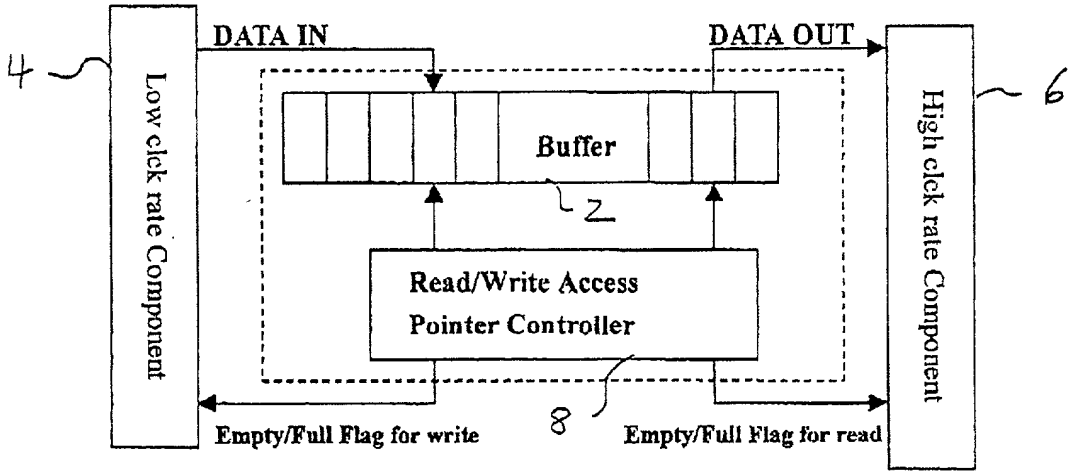

Fig. 1 (Prior art)

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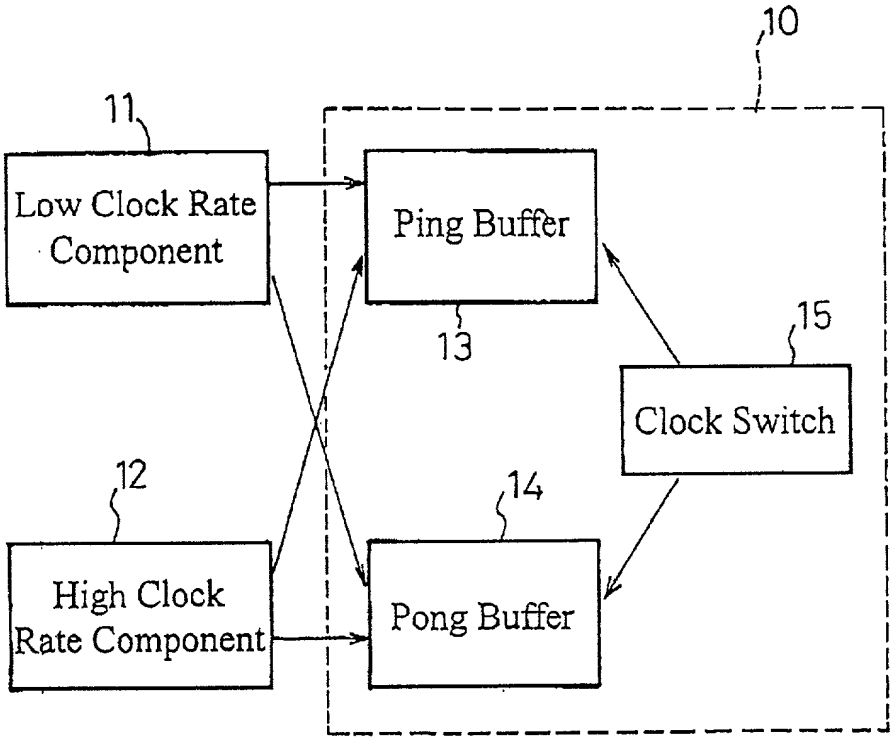

Fig. 2

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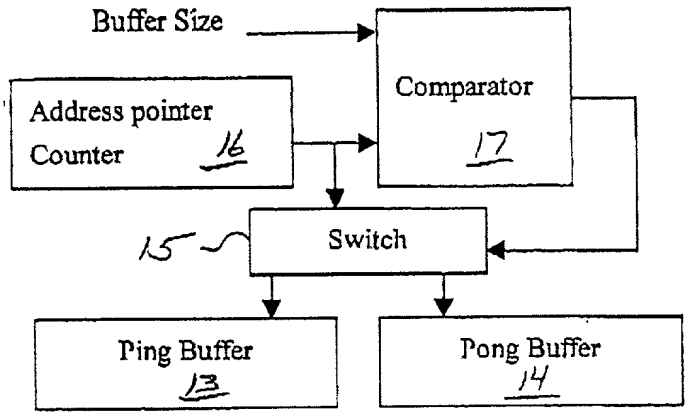

Fig. 3

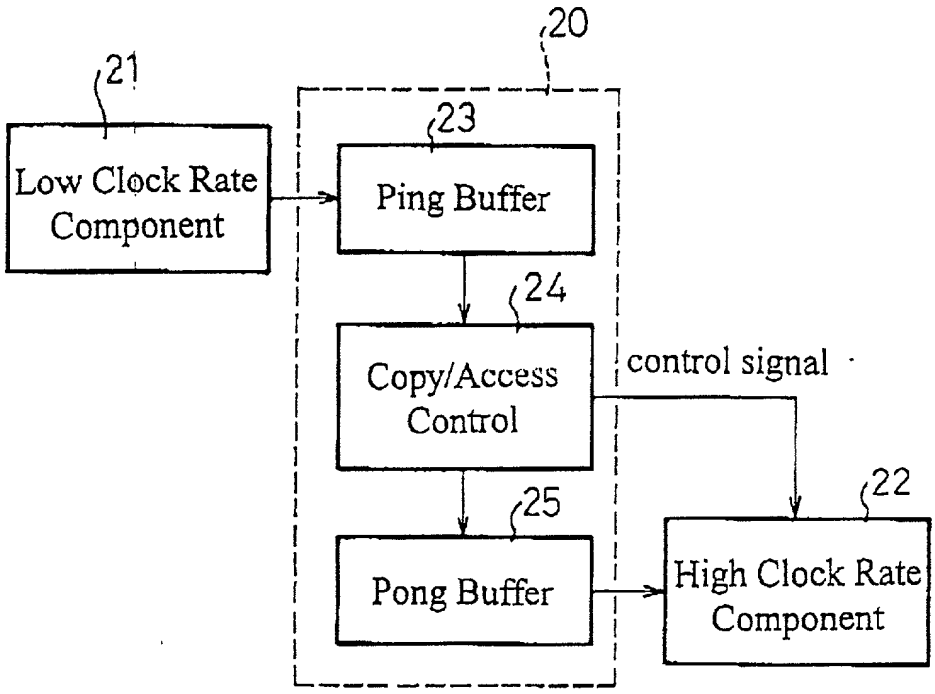

Fig. 4

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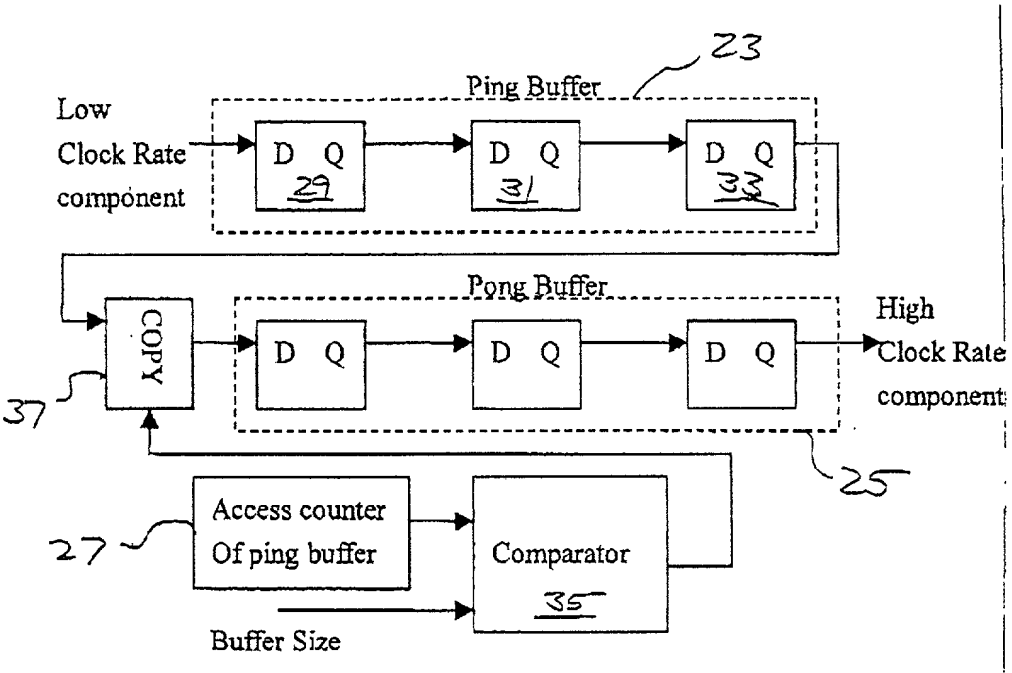

Fig. 5

TI Docket No
TI-29058

APPLICATION FOR UNITED STATES PATENT
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As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: INTERFACE BETWEEN DIFFERENT CLOCK RATE COMPONENTS

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

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DATE: 3/24 '00	DATE:	DATE: